In the claims:

Please enter the amendments as indicated below.

1. (Currently Amended) A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time event at the personal computer indicating a request to process the real time data;

determining whether the real-time event has a higher priority than a first non-real time event being processed at the personal computer; and

processing the real-time data [real-time event] if the real-time event has a higher priority than the first non-real time event.

2. (Currently Amended) The method of claim 1 further comprising continuing to process the first non-real time event if the real-time event does not have a higher priority than the first event.

3. (Currently Amended) The method of claim 1 further comprising:

saving the state of the first non-real time event at the personal computer prior to processing the real-time event; and

processing the [prior] first non-real time event after processing of the real-time event has been completed.

4. (Currently Amended) The method of claim 1 further comprising:

receiving a second non-real time event while processing the real-time event; and

determining whether the second non-real time event has a higher priority than the real-time event.

5. (Currently Amended) The method of claim 4 further comprising:

continuing the processing of the real-time event if the second non-real time event does not have a higher priority than the [second] real time event.

6. (Currently Amended) The method of claim 4 further comprising:

terminating the processing of the real-time event if the second non-real time event has a higher priority; and

processing the second non-real time event.

7. (Currently Amended) A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), coupled to the bus, [that operates according to a general purpose operating system, and processes real-time data received at the computer system] to generate real-time events upon receiving real-time analog data and to process the real-time analog data if the real-time event has a higher priority than a non-real-time event.

8. (Currently Amended) The computer system of claim 7 wherein the CPU comprises:

a timer to generate timing signals at predetermined time intervals; and

an event mechanism coupled to the timer to generate the real time events.

9. (Currently Amended) The computer system of claim 8 wherein the CPU further comprises an event handler coupled to the event mechanism to process the real-time events.

10. (Original) The computer system of claim 9 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data.

11. (Currently Amended) The computer system of claim 9 wherein the event mechanism determines the relative priority between the real-time events and the non-real-time events.

12. (Original) The computer system of claim 11 wherein the CPU further comprises an analog to digital converter coupled to the register.

13. (Currently Amended) A central processing unit (CPU) comprising:

a timer to generate timing signals at predetermined time intervals;

an event mechanism coupled to the timer to generate real time events in response to receiving the timing signals and real-time data; and

an event handler coupled to the event mechanism to process the real-time events received from the event mechanism upon determining the relative priority between the real-time events and non-real-time events.[,

the CPU operating according to a general purpose operating system.]

14. (Previously Amended) The computer system of claim 13 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data.

15. (Previously Amended) The computer system of claim 14 wherein the event handler verifies whether there is data stored in register upon detecting a real-time event and determines the priority of the real-time event relative to other interrupts received.

16. (Previously Amended) The computer system of claim 14 wherein the CPU further comprises an analog to digital converter coupled to the register.

17. (Previously Added) The method of claim 1 wherein receiving the real-time analog data comprises:

converting the real-time analog data to digital data; and

storing the digital data at a register.